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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,540	12/28/2005	Vasanth R. Gaddam	US030205US2	5888

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EXAMINER	
WYLLIE, CHRISTOPHER T	

ART UNIT	PAPER NUMBER
2465	

NOTIFICATION DATE	DELIVERY MODE
08/19/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/562,540	GADDAM ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER WYLLIE	2465	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,2,4-9,11-13,15,16,18-20 and 22-27* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *22,26 and 27* is/are allowed.

7)☒ Claim(s) *1,2,4-9,11-13,15,16,18-20 and 23-25* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *28 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. This action is responsive to the communication received June 1st, 2011. Claims 1, 15, 18, 22, and 25 have been amended. Claims 3, 10, 14, 17, and 21 have been canceled. Claims 1-2, 4-9, 11-13, 15-16, 18-20, and 22-27 have been entered and are presented for examination.

2. Application 10/562,540 is a 371 of PCT/IB04/51037 (06/28/2004) and claims benefit to Provisional Application 60/483,792 (06/30/2003).

3. Applicant's arguments, filed June 1st, 2011, have been fully considered, but deemed moot in view of the new grounds of rejection.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1,4-5, 7-8, 11-12, 14-15, 18-19, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Birru et al. (US 7,111,221) in view of Gaddam et al. (US 2002/0191712).

Regarding claim 1, Strolle et al. discloses a packet formatter **(see Figure 3, Demodulator/Decoder 314)** comprising: a first processing block capable of receiving a dual bit stream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signal is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet steam and a robust packet stream])**, the robust stream having associated therewith header bytes and parity bytes **(paragraph 0030, lines 3-9 [parity bytes are added to the robust data packet and to**

ensure backwards compatibility header bytes for the robust packet are encoded with a NULL packet header and encoded as normal data; therefore the robust data has header bytes and parity bytes]); in response to which the first processing block removes the header bytes and parity bytes from dual bit stream signal to output a first output signal **(paragraph 0085, lines 5-12 [header bytes are stripped and then RS decoder removes the parity bytes])**. Strolle et al. does not explicitly disclose that the locations of the parity bytes a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bit stream signal and a second processing block capable of determining the locations of the parity bytes within the robust packet according to the robust packet's position within its frame. Birru et al. suggests such a feature **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of Strolle et al. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

The references as applied above do not disclose a third processing block capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Gaddam et al. discloses such a feature **(paragraph 0054 [discloses for robust streams, the information bit need only be placed in the robust byte at the desirable bit position for robust trellis encoding and symbol mapping. With greater particularity, at the MPEG packet level, for each robust packet carrying information, two packets are generated: one being the information carrier packet, and the other functioning as a placeholder packet. In the packet formatter 330, only the information carrier packet (not the placeholder packet) is processed. Particularly as shown in FIG. 6, the packet formatter generates two robust bytes (packets) 332a, 332b for each byte 331 of each packet received from the robust stream. The packet formatter 330 will generate two identical bits, e.g., bits 333, 334 corresponding to each information bit 335 of each input byte processed; Paragraph 0068 further discloses the Packet Formatter block 555 reformats the robust bit-stream packets. When NRS=0, it transforms two NS packets into one packet for input to the RS decoder block 560])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Gaddam et al. into the system of Strolle et al. The method of Gaddam et al. can be implemented by incorporating a

packet formatter block in the transmitter. The motivation for this is to enable the transmitter to reformat the robust stream.

Regarding claim 4, the references as applied above disclose all the recited subject matter in claim 1. However Birru et al. further discloses that the second processing block is further capable of determining the locations of said header bytes in said robust stream **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding claim 5, Strolle et al. further discloses that the second processing block contains a look-up table **(paragraph 0079, lines 10-16 [a complete map of VSB symbols indicating whether each symbol is robust or normal is assembled in block 323])**. Strolle et al. does not explicitly disclose that the locations of the parity

bytes within each robust packet being dependent upon a position of a robust packet within a frame of packets. However, Birru et al. suggests such a feature **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding claim 7, the references as applied above do not disclose a signal comprising the second output signal from the data path of the packet formatter. However, Gaddam et al. further discloses such a feature **(see Figure 10])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Gaddam et al. into the system of the references as applied above. The method of Gaddam et al. can be implemented by incorporating a decode sync header block in the receiver. The motivation for this is

to enable the equalizer to determine the locations of the robust packets in a frame and using the decode sync header block to identify the parity bytes within the robust packet.

Regarding claim 8, Strolle et al. discloses a television receiver capable of receiving a dual bit stream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signal is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet stream from the digital television receiver and a robust packet stream])**, the robust stream having associated therewith header bytes and parity bytes **(paragraph 0030, lines 3-9 [parity bytes are added to the robust data packet and to ensure backwards compatibility header bytes for the robust packet are encoded with a NULL packet header and encoded as normal data; therefore the robust data has header bytes and parity bytes])**, a method of formatting packets of said dual bit stream signal comprising the steps of: receiving in a packet formatter said dual bit stream signal **(paragraph 0078, lines 2-8 [the enhances signal is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet steam and a robust packet stream])**, removing the header bytes and parity bytes the dual bit signal to thereby produce a first output signal **(paragraph 0085, lines 5-12 [header bytes are stripped and then RS decoder removes the parity bytes])**. **])**. Strolle et al. does not explicitly disclose that the locations of the parity bytes a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bit stream signal and a second

processing block capable of determining the locations of the parity bytes within the robust packet according to the robust packet's position within its frame. Birru et al. suggests such a feature **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of Strolle et al. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

The references as applied above do not disclose a third processing block capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Gaddam et al. discloses such a feature **(paragraph 0054 [discloses for robust streams, the information bit need only be placed in the robust byte at the desirable bit position for robust trellis encoding and symbol mapping. With greater particularity, at the MPEG packet level, for each robust packet carrying information, two packets are**

generated: one being the information carrier packet, and the other functioning as a placeholder packet. In the packet formatter 330, only the information carrier packet (not the placeholder packet) is processed. Particularly as shown in FIG. 6, the packet formatter generates two robust bytes (packets) 332a, 332b for each byte 331 of each packet received from the robust stream. The packet formatter 330 will generate two identical bits, e.g., bits 333, 334 corresponding to each information bit 335 of each input byte processed; Paragraph 0068 further discloses the Packet Formatter block 555 reformats the robust bit-stream packets. When NRS=0, it transforms two NS packets into one packet for input to the RS decoder block 560]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Gaddam et al. into the system of Strolle et al. The method of Gaddam et al. can be implemented by incorporating a packet formatter block in the transmitter. The motivation for this is to enable the transmitter to reformat the robust stream.

Regarding claim 11, the references as applied above disclose all the recited subject matter in claim 8. However Birru et al. further discloses that the second processing block is further capable of determining the locations of said header bytes in said robust stream **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This**

indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding claim 12, Strolle et al. further discloses that the second processing block contains a look-up table **(paragraph 0079, lines 10-16 [a complete map of VSB symbols indicating whether each symbol is robust or normal is assembled in block 323])**. Birru et al. further discloses that the locations of the parity bytes within each robust packet being dependent upon a position of a robust packet within a frame of packets**(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding claim 14, the references as applied above do not disclose a signal comprising the second output signal from the data path of the packet formatter. However, Gaddam et al. further discloses such a feature **(see Figure 10])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Gaddam et al. into the system of the references as applied above. The method of Gaddam et al. can be implemented by incorporating a decode sync header block in the receiver. The motivation for this is to enable the equalizer to determine the locations of the robust packets in a frame and using the decode sync header block to identify the parity bytes within the robust packet.

Regarding claim 15, Strolle et al. discloses a television receiver **(see Figure 3, Digital Television Receiver 316)** comprising: receiver front-end circuitry **(see Figure 3, Demodulator/Decoder 314)** capable of receiving and down-converting a dual bit stream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signal is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet steam and a robust packet stream])** having

associated therewith header bytes and parity-bytes **(paragraph 0030, lines 3-9 [parity bytes are added to the robust data packet and to ensure backwards compatibility header bytes for the robust packet are encoded with a NULL packet header and encoded as normal data; therefore the robust data has header bytes and parity bytes])**, the receiver front-end circuitry producing a baseband signal; and a packet formatter comprising: a first processing block capable of receiving said standard stream and said robust stream associated with said baseband signal **(see Figure 3A, Equalizer 326 [the equalizer receives the normal/Robust packet])**; in response to which the first processing block removes from the header bytes and parity bytes from dual bit stream signal to output a first output signal **(paragraph 0085, lines 5-12 [header bytes are stripped and then RS decoder removes the parity bytes])**; a robust de-interleaver capable of receiving the second output signal and deinterleaving data in the robust stream to output a third output signal **(see Figure 3A, De-interleaver 330)**; a Reed-Solomon decoder capable of receiving the third output signal and decoding data in the third output signal to output a fourth output signal **(see Figure 3A, RS Decoder 332)**; and a de-randomizer capable of receiving the fourth output signal and de-randomizing bytes associated with said standard stream and bytes associated with said robust stream **(see Figure 3A, De-randomizer 334)**. Strolle et al. does not explicitly disclose that the locations of the parity bytes within each robust packet being dependent upon a position of a robust packet within a frame of packets in the dual bit stream signal and a second processing block capable of determining the locations of the parity bytes within the robust packet according to the robust packet's position within

its frame and a forward error correction section capable of receiving said baseband signal from said receiver front-end circuitry wherein said forward error correction section comprises a packet formatter. Birru et al. suggests such a feature **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of Strolle et al. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

The references as applied above do not disclose a second processing block capable of receiving said first output signal and removing there from duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Gaddam et al. discloses such a feature **(paragraph 0054 [discloses for robust streams, the information bit need only be placed in the robust byte at the desirable bit position for robust trellis encoding and symbol mapping. With greater particularity, at the MPEG packet level, for each robust packet carrying information, two packets are**

generated: one being the information carrier packet, and the other functioning as a placeholder packet. In the packet formatter 330, only the information carrier packet (not the placeholder packet) is processed. Particularly as shown in FIG. 6, the packet formatter generates two robust bytes (packets) 332a, 332b for each byte 331 of each packet received from the robust stream. The packet formatter 330 will generate two identical bits, e.g., bits 333, 334 corresponding to each information bit 335 of each input byte processed; Paragraph 0068 further discloses the Packet Formatter block 555 reformats the robust bit-stream packets. When NRS=0, it transforms two NS packets into one packet for input to the RS decoder block 560]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Gaddam et al. into the system of Strolle et al. The method of Gaddam et al. can be implemented by incorporating a packet formatter block in the transmitter. The motivation for this is to enable the transmitter to reformat the robust stream.

Regarding claim 18, the references as applied above disclose all the recited subject matter in claim 15. However Birru et al. further discloses that the second processing block is further capable of determining the locations of said header bytes in said robust stream **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This**

indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding claim 19, Strolle et al. further discloses that the second processing block contains a look-up table **(paragraph 0079, lines 10-16 [a complete map of VSB symbols indicating whether each symbol is robust or normal is assembled in block 323])**. Birru et al. further discloses that the locations of the parity bytes within each robust packet being dependent upon a position of a robust packet within a frame of packets**(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding clam 23, the references as applied above disclose all the claimed subject matter recited in claim 1. However, Birru et al. further discloses that locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**, and wherein the second processing block is capable of determining the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100,**

152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding clam 24, the references as applied above disclose all the claimed subject matter recited in claim 8. However, Birru et al. further discloses that locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.]**), and wherein the second processing block is capable of determining the locations of the parity bytes within each of the first and second robust

packets according to the first and second robust packets' corresponding positions within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

Regarding clam 25, the references as applied above disclose all the claimed subject matter recited in claim 15. However, Birru et al. further discloses that locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity**

byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.]), and wherein the second processing block is capable of determining the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame **(column 12, lines 19-42 [positions of the parity bits are determined based on the location of the packet; as an example, substituting k=0 and n=187 to 206 will give parity byte locations for packet 0 as 202, 47, 99, 151, 203, 48, 100, 152, 204, 49, 101, 153, 205, 50, 102, 154, 206, 51, 103, 155. This indicates that the parity byte PB0 should be placed at location 202 in packet 0 so that its position after the interleaver is 187 in packet 0. Similarly, parity byte PB1 has to be placed at location 47 and so on.])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Birru et al. into the system of the references as applied above. The method of Birru et al. can be implemented by incorporating a packet de-formatter unit in the receiver. The motivation for this is to determine the location of the parity bits according to the setup of the packet formatter unit in the transmitter.

9. Claims 2, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Birru et al. (US 7,111,221) in view of

Gaddam et al. (US 2002/0191712)as applied to claim 1,8, and 15 above, and further in view of Hurst, Jr. (US 6,034,731).

Regarding claim 2, the references as applied above disclose all the claimed subject matter recited in claim 1, but do not disclose that the packet formatter passes bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

Regarding claim 9, the references as applied above disclose all the claimed subject matter recited in claim 8, but do not disclose that the packet formatter passes bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

Regarding claim 16, the references as applied above disclose all the claimed subject matter recited in claim 15, but do not disclose that the packet formatter passes bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

10. Claims 6, 13, and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Birru et al. (US 7,111,221) in view of

Gaddam et al. (US 2002/0191712) as applied to claim 5, 12, and 19 above, and further in view of Fimoff (US 2001/0055342).

Regarding claim 6, the references as applied above disclose all the claimed subject matter recited in claim 5, but do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Regarding claim 13, the references as applied above disclose all the claimed subject matter recited in claim 12, but do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the**

data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Regarding claim 20, the references as applied above disclose all the claimed subject matter recited in claim 19, but do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Allowable Subject Matter

11. Claims 22 and 26-27 are allowed.

Response to Arguments

12. Applicant's arguments, filed June 1st, 2011, have been fully considered, but deemed moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER WYLLIE whose telephone number is (571)270-3937. The examiner can normally be reached on Monday through Friday 8:30am to 6:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/MARSHA D. BANKS HAROLD/
Supervisory Patent Examiner, Art Unit 2465

/Christopher T. Wyllie/
Examiner, Art Unit 2465